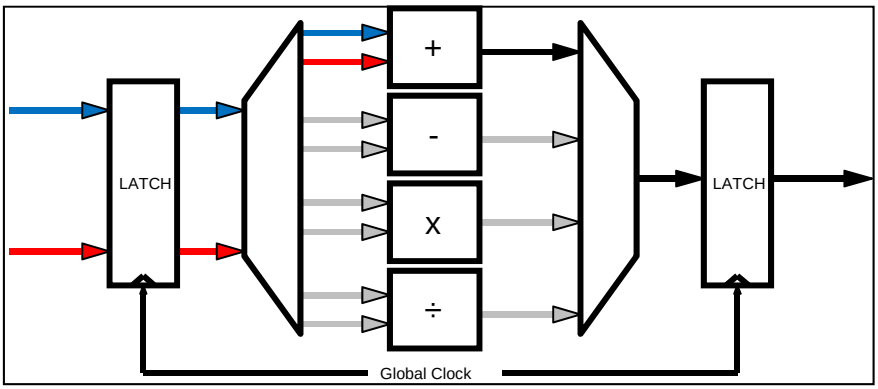
The Institution of Engineering and Technology

EC³ Section

Squeezing the remaining nanoseconds out of digital logic

Des Howlett



The speed of digital logic is governed by three main aspects: process technology, design techniques and the basic laws of physics. Technology is continually being improved, but the one place that Engineers have the most influence is the design methodology. They constantly strive to reduce the logic delays between clocked elements in order to get the highest possible system speed.

This talk will show a means by which the delays can be reduced to just one or two gates by blending synchronous and asynchronous techniques. In doing so, circuits can remain fully synchronous, use standard design tools (including FPGAs) yet allow functions to take only the amount of time that they actually require.

This event is free of charge and open to all, with refreshments at 19.00.

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Thursday 26 January 2012 19.00 for 19.30

Palmer Building, University of Reading RG6 6UR

For directions please visit http://www.reading.ac.uk/about/find/about-findindex.aspx